

FIG. 1

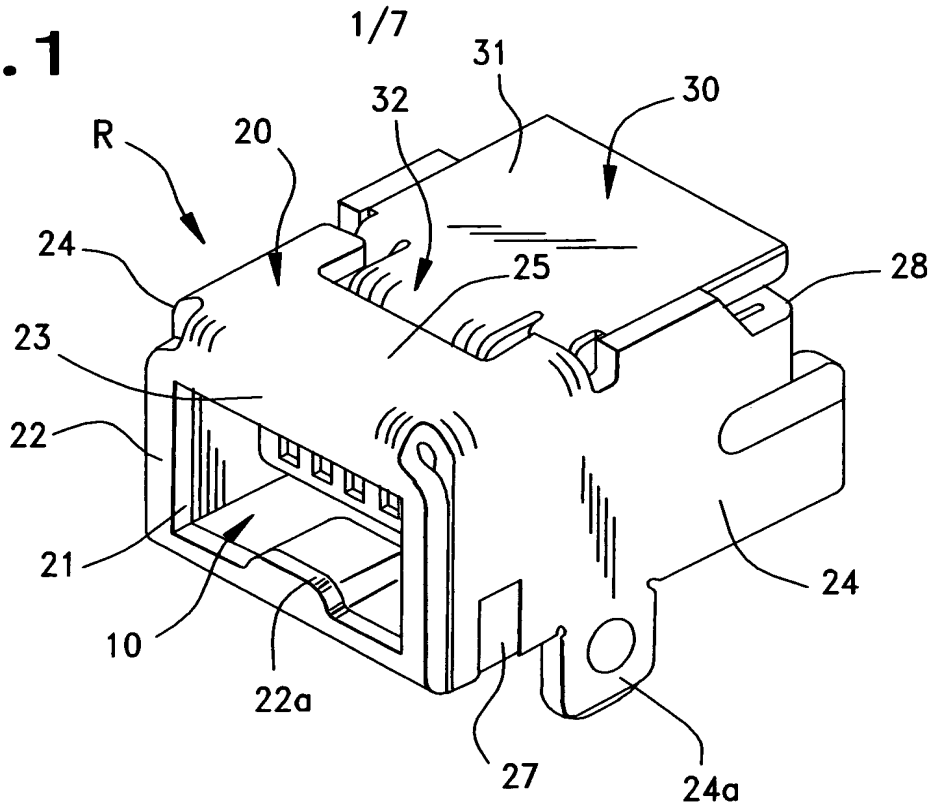
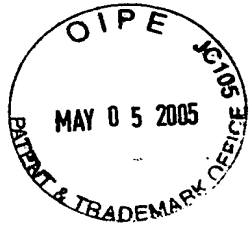
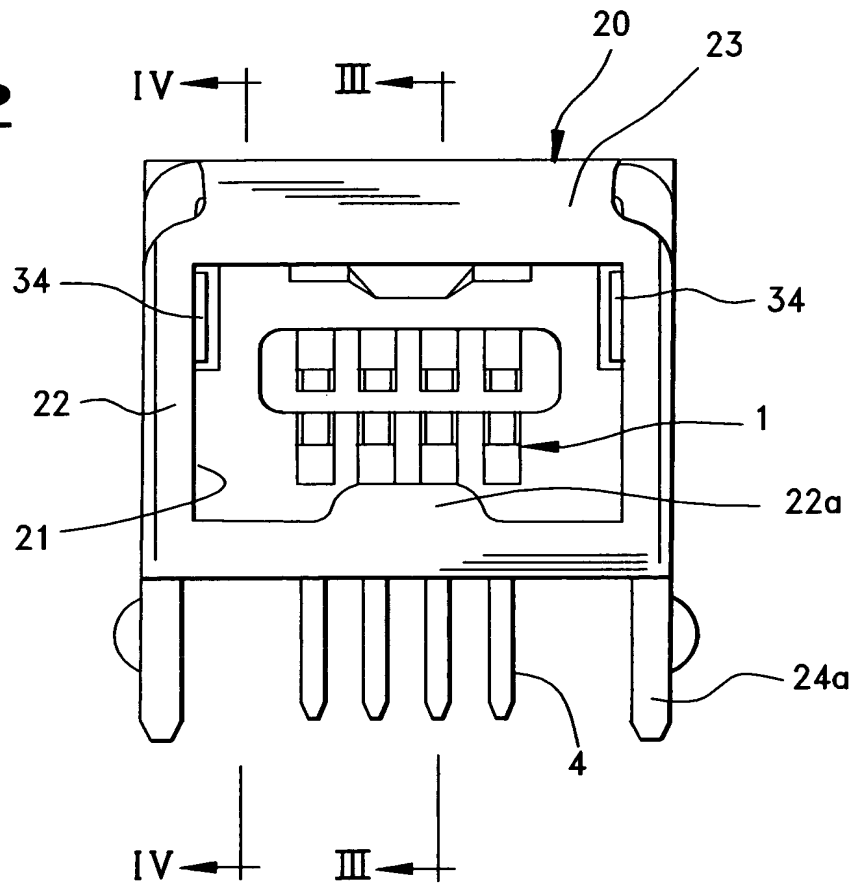
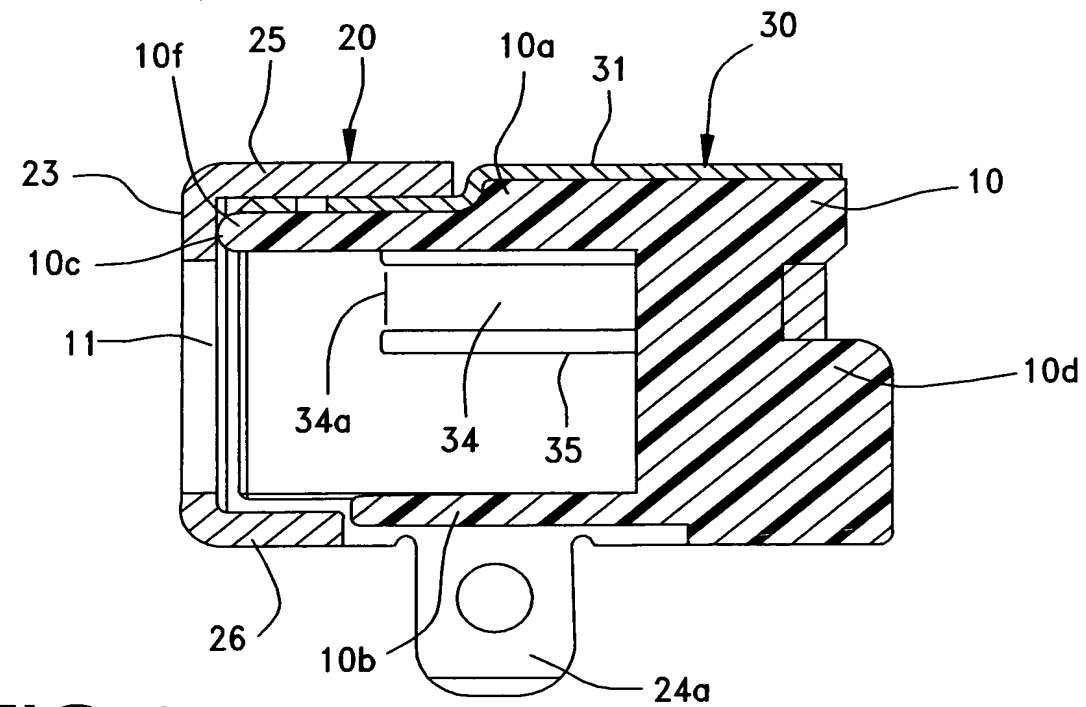


FIG. 2



**FIG. 3**



**FIG.4**

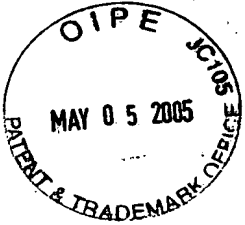


FIG. 5

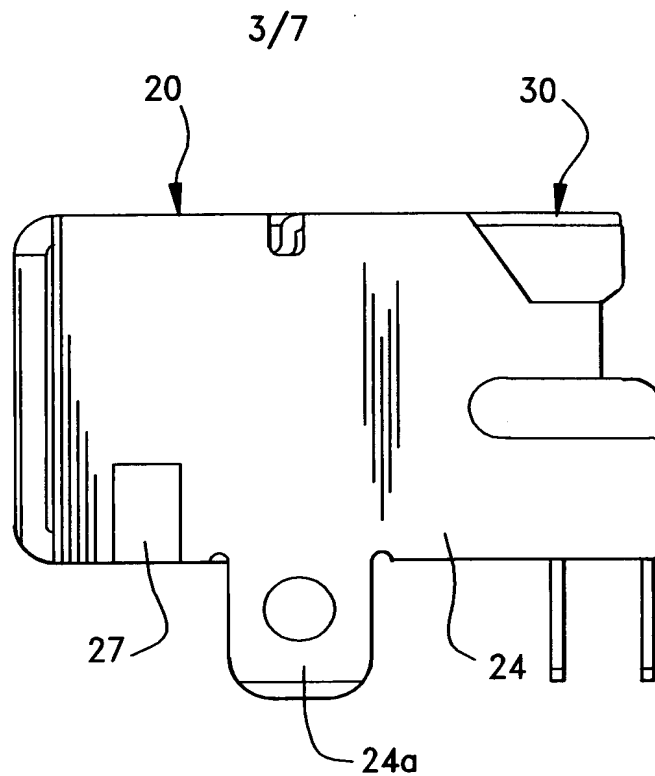


FIG. 6

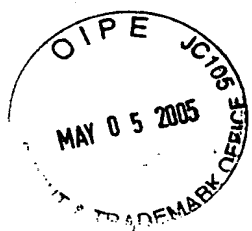
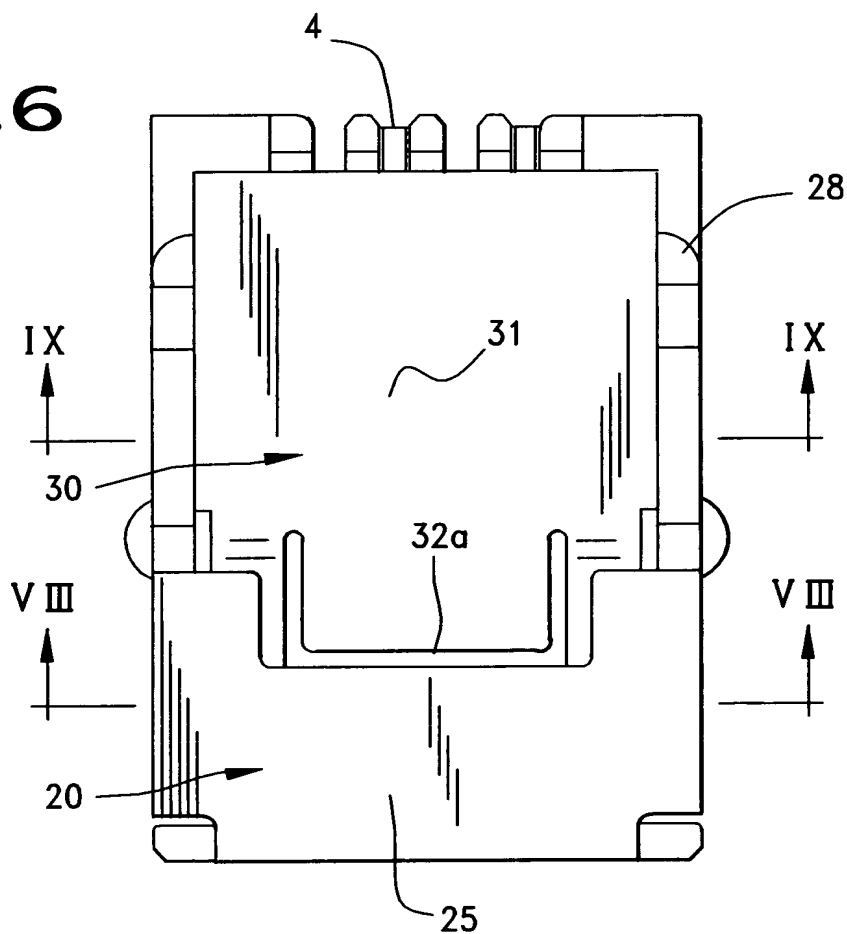


FIG. 7

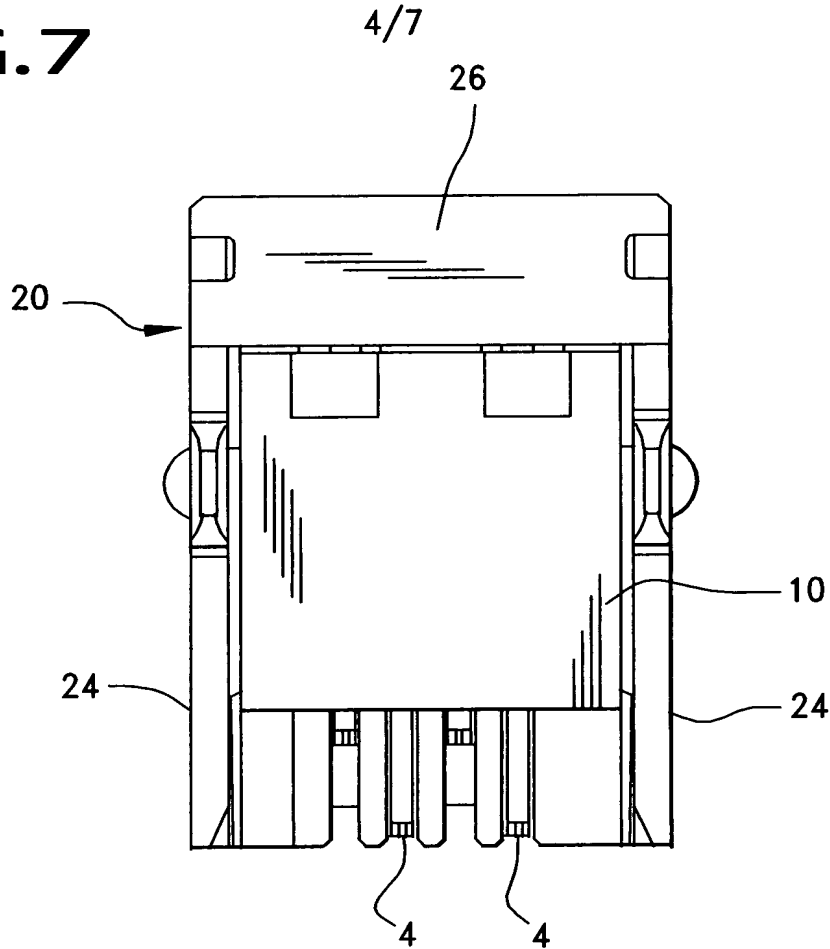
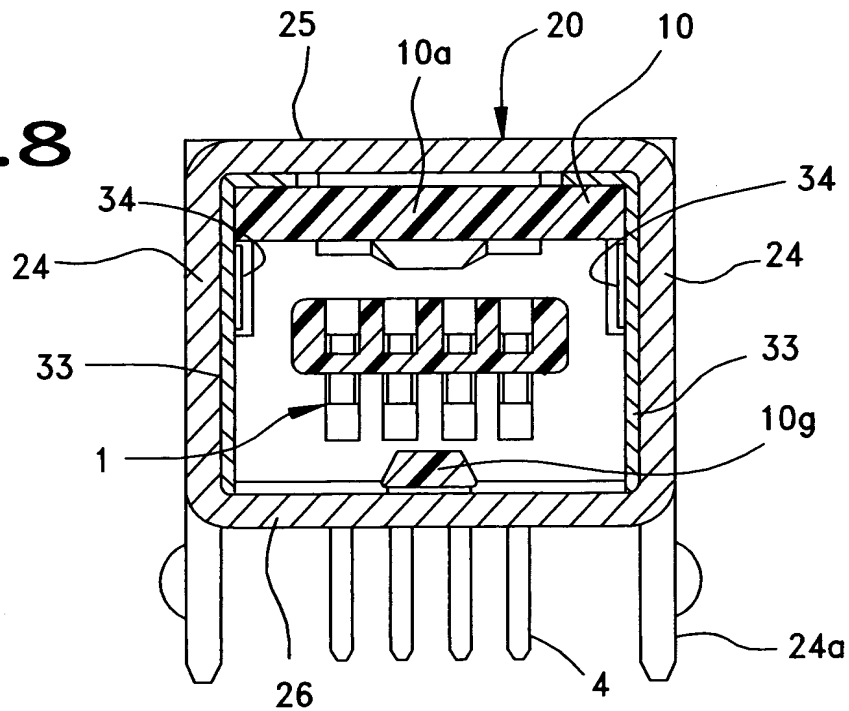
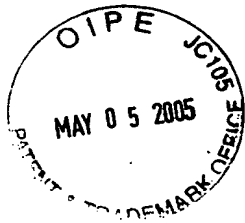


FIG. 8



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**G.10**

This diagram shows a plan view of a second embodiment of a semiconductor device. It features a central rectangular region 22 containing a square area 22a. This central region is surrounded by a frame-like structure 23. On the left side, there is a vertical strip 26 with two rectangular protrusions 27, each having a top surface 105. The bottom of this strip is labeled 21. The right side of the device is defined by a boundary 24, which includes two circular features 24a. A horizontal strip 25 is located between the central region 22 and the right boundary 24. On the right side, there are two rectangular protrusions 28, each with a top surface 106. The entire device is labeled 102. Dashed lines 101 and 103 indicate internal boundaries or layers. The label 104 is located within the central region 22.

FIG. 11

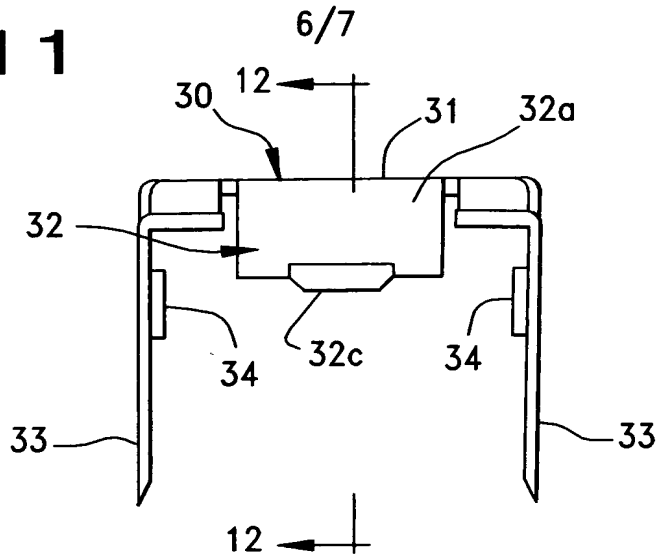


FIG. 12

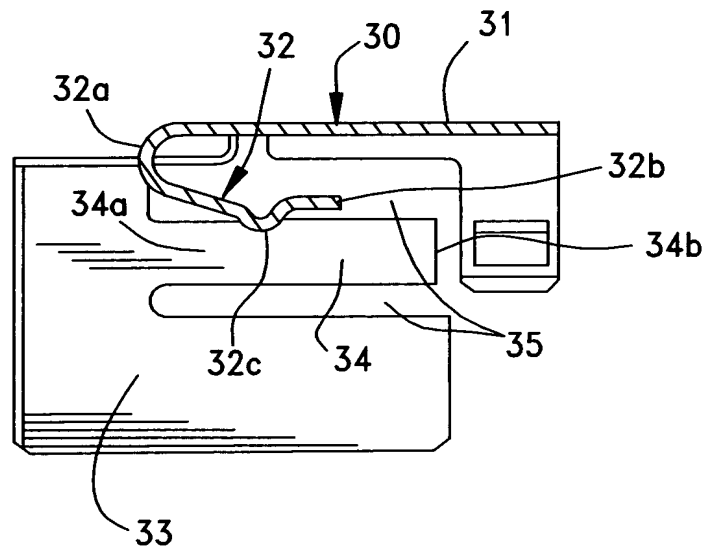
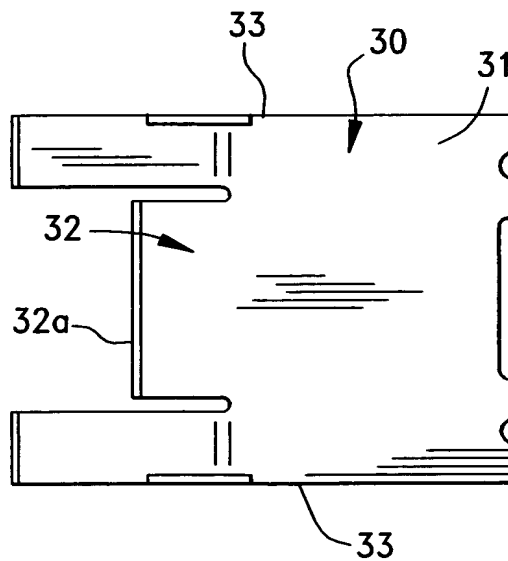
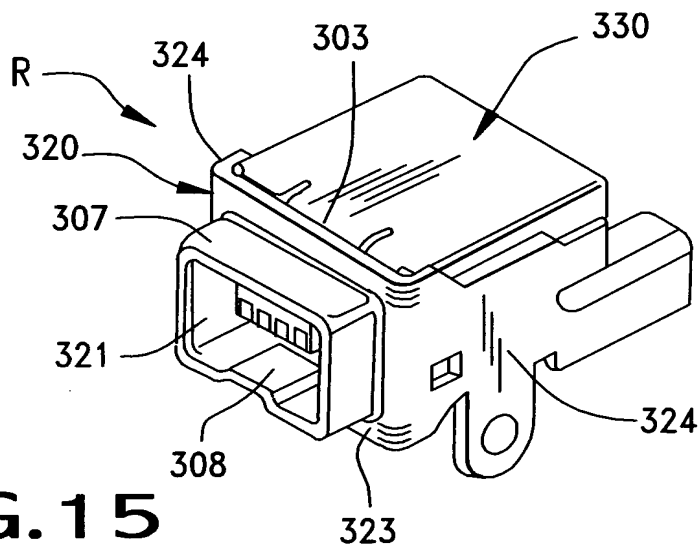
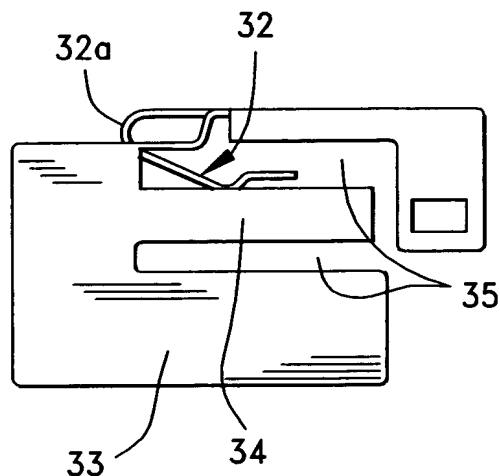


FIG. 13

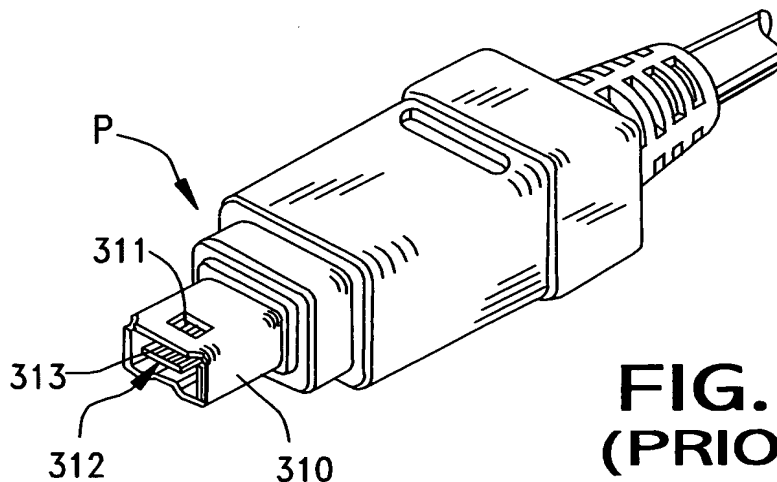


**FIG. 14**

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**FIG. 15  
(PRIOR ART)**



**FIG. 16  
(PRIOR ART)**